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High Performance InP Laser Technology Supporting RF Silicon Photonics Integration

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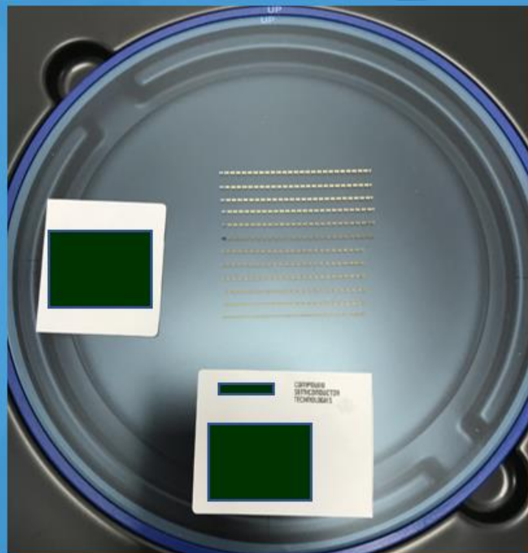
Presentation Outline

- CST Global Backgrounder & Device Technology
- CST 'InP100' Platform
  - Platform Features & Supported Devices
    - *DFB lasers for rf photonics*
    - 1270nm GPON DFB Lasers
    - 28Gbs^{-1} Direct Mod Lasers
    - Wide operating temperature range DFBs
    - High Power C-band DFB for LIDAR
    - Reflective SOAs for tuneable lasers.
  - Platform Summary and Roadmap
- Silicon Photonics Overview & Landscape
  - Applications
  - III-V Hybrid Integration Technology
- Connection between 'InP100' and Silicon Photonics
  - Mechanical Integration
  - Accessing InP100 with Cadence Design Tools
- Final Summary

COMPOUND SEMICONDUCTOR TECHNOLOGIES

CST Public

- CST Global - Designing and Manufacturing III-V Photonic Devices in the UK since 1999



COMPOUND SEMICONDUCTOR TECHNOLOGIES

20,000 sq-ft cleanroom III-V Wafer Fab facility (< Class 50.) located in Blantyre, UK.

Lasers, detectors, modulators, amplifiers on InP, GaAs, GaSb and GaN wafers.

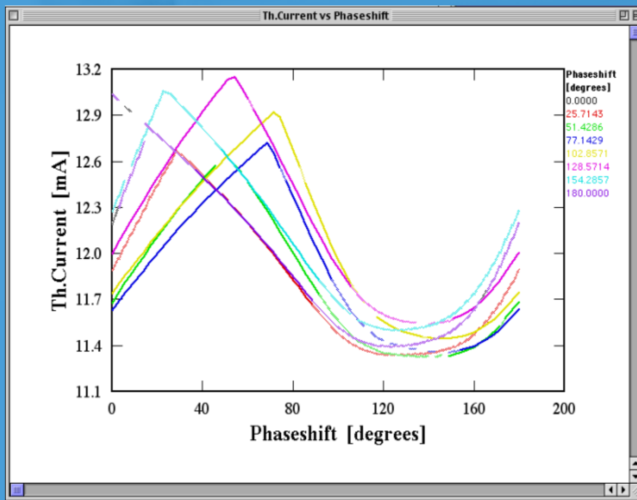
Flexible output format from processed wafers through to fully characterised assembled Chip-On-Submount.

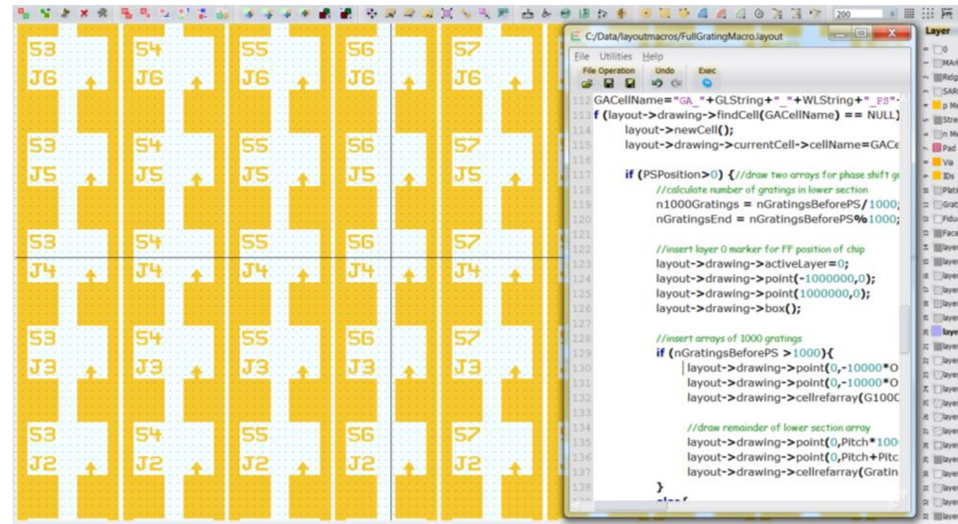
Standard output:- Known-Good-Die-On-Tape (KGDOT)

CST Public

- Design and Modelling

- Full in-house design capability to translate customer requirements into full chip designs.
  - AlInGaAs and InGaAsP SMQW active region modelling.
  - Full device modelling using commercial and bespoke software packages.
  - Key strength in AlInGaAs DFB laser design for high-speed and high-power uncooled operation.
  - Designs optimised for high-reliability performance.
  - Scripted GDS CAD Layout with auto DRC.

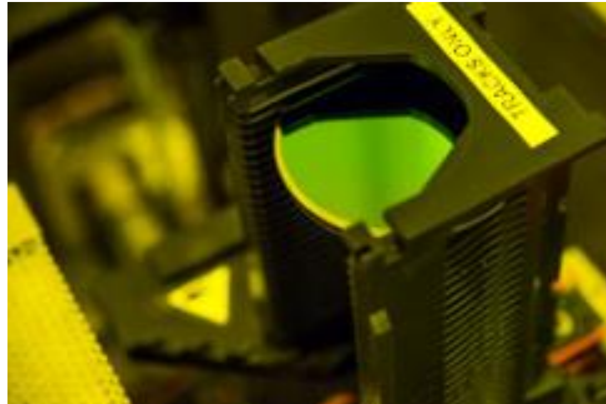




COMPOUND SEMICONDUCTOR TECHNOLOGIES

Wafer Fab and Test

- Processing up to 100mm wafer sizes
- Contact and stepper based lithography (up to 20 layers)
- Automated backend (post-fab) processing
- High volume test capacity (2M lasers/month)



COMPOUND SEMICONDUCTOR TECHNOLOGIES

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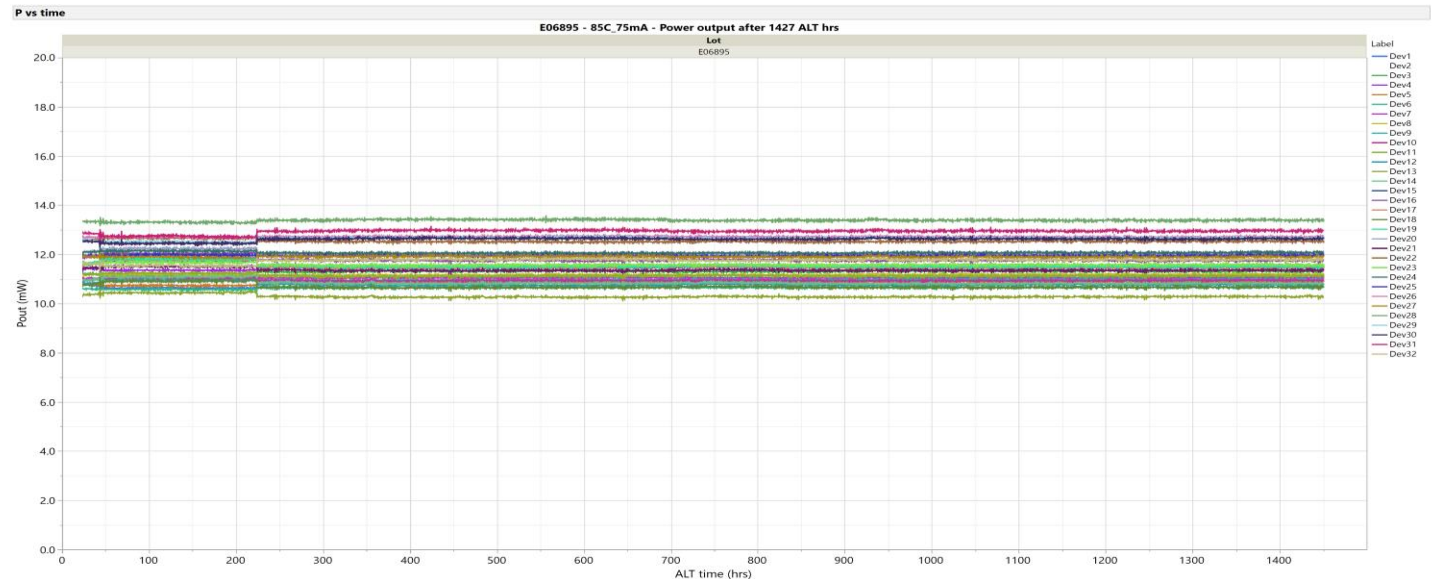
- Chip Reliability and Qualification

COMPOUND SEMICONDUCTOR TECHNOLOGIES

- In-house capability to perform:
  - HTOL and ALT testing to GR468. 2,000hrs, 5khrs &10khrs test durations.
  - Damp-heat testing (eg 85C/85%)
  - Low and High temperature storage.
  - Detailed analysis, reliability and qual reports.



CST Public

Backgrounder Summary

- 20 year history designing and manufacturing III-V photonic devices
- Processing around 1000 wafers per year. Capacity of fab significantly higher.
  - Historic mix of InP (50%), GaAs (45%), GaSb (5%), GaN
- Traditionally manufacturing a very diverse mix of devices.
- Established InP laser supplier in volume PON markets shipping around 1M lasers (DFBs + FPs) per month
  - *Around 45 Million lasers in the field.*

- **Recent dramatic increase in InP laser demand driven by emerging applications and Silicon Photonics integration.**
- **Implementation of "Platform Technology" approach necessary to increase standardisation and improve productivity.**

COMPOUND SEMICONDUCTOR TECHNOLOGIES

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CST InP100 Platform

COMPOUND SEMICONDUCTOR TECHNOLOGIES

Key features

- 100mm wafer size. Up to 125,000 die sites / wafer
- AlInGaAs and InGaAsP active regions. (1250nm to >1650nm)
- Coplanar ridge waveguide process architecture
- Ebeam lithography DFB gratings
- On-wafer facet etch and optical coatings
- Non-hermetic compatible
- Known-good die-on-tape delivery format
- Optimised architecture for SiPh flip-chip bonding
- Scalable to high volume

Supported Devices

- DFB Lasers
  - Modulation rates from CW to $28GBs^{-1}$
  - Rated power from 10mW to 100mW+
  - Very broad operating temperature range (-50°C to +95°C)
  - Narrow linewidth (<300kHz)
- Reflective SOAs for external cavity tuneable lasers
- MOPAs, EAMs and EMLs
- Single and array output format

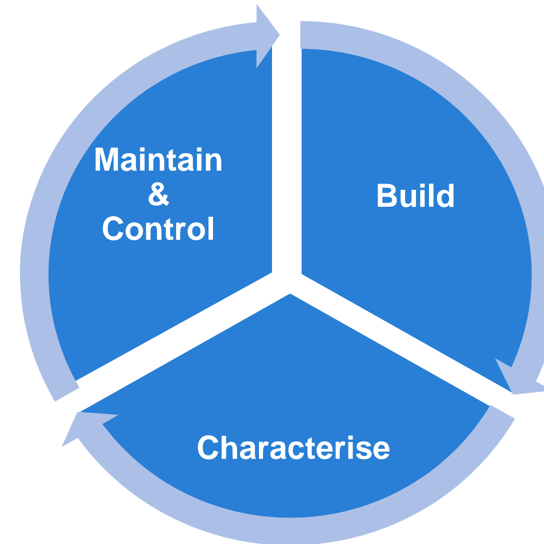
CST Public

- CST InP100 Platform

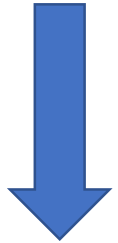
COMPOUND SEMICONDUCTOR TECHNOLOGIES

- Key Benefits
  - productivity
  - efficiency
  - stability

- Data acquisition
- Controls and monitors
- Rigorous process and tolerances
- SPC and PCMs
- >5Gb data per wafer



Customer



- Faster cycle times
- Consistent quality

- Roadmap
  - 150mm wafer size
  - AuSn solder pads
  - Stealth dicing
  - Auto-Optical Inspection (AOI)

CST Public

- CST InP100 Platform

COMPOUND SEMICONDUCTOR TECHNOLOGIES

- Device Examples

CST Public

• DFB Lasers for rf photonics

Innovate-UK Project "WiPhi"

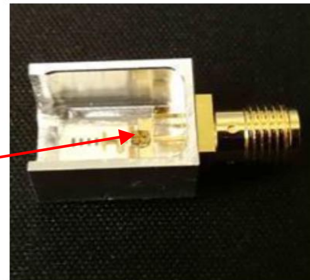
High performance wireless/photonic interfaces for 60 GHz radio over fibre applications"

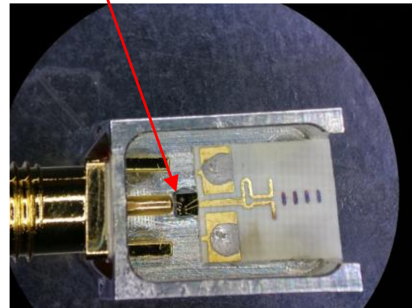
COMPOUND SEMICONDUCTOR TECHNOLOGIES

- Objective was to develop High-Speed DFB lasers for wireless to optical domain (Radio over Fibre) signal conversion.
- This was accomplished by direct modulation of the DFB laser by RTD amplified 1Gbs^{-1} baseband signals.

Packaged version of 60 GHz wireless transmitter:

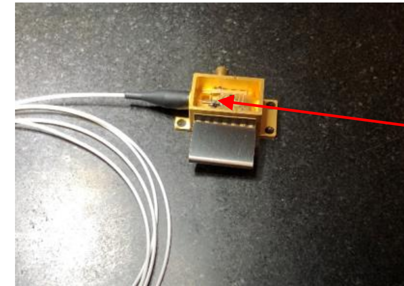
60 GHz RTD oscillator

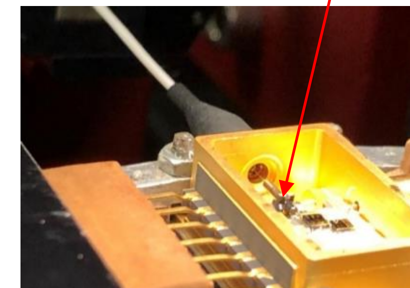


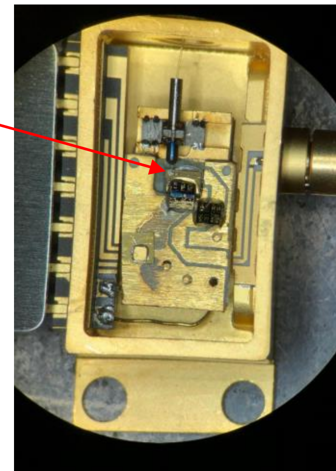


Butterfly package version of 10 Gbps RoF transducer

CST 10 Gbps DFB laser







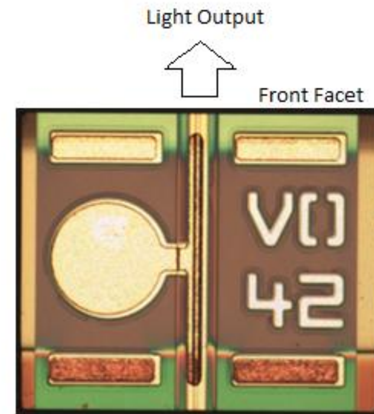
CST Public

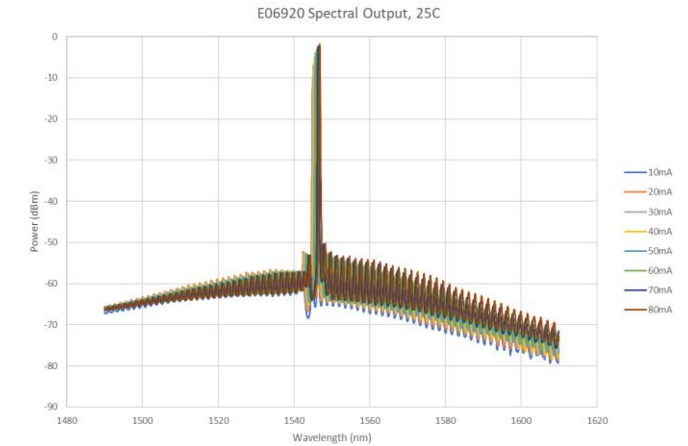
• DFB Lasers for rf photonics

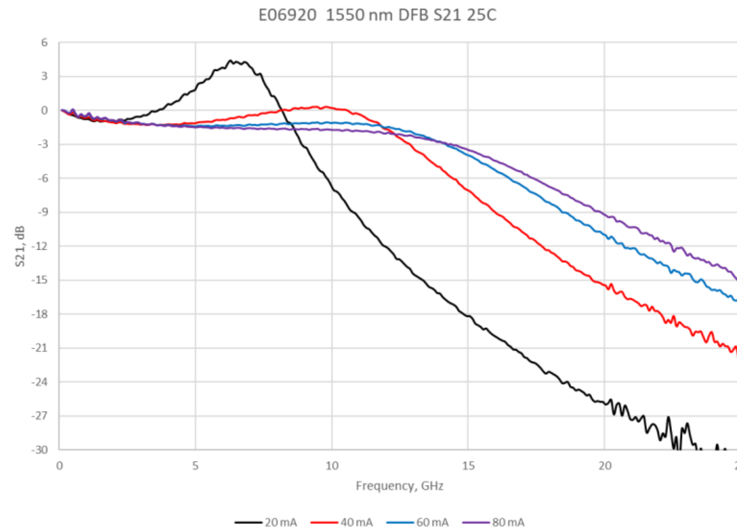
Innovate-UK Project "WiPhi"

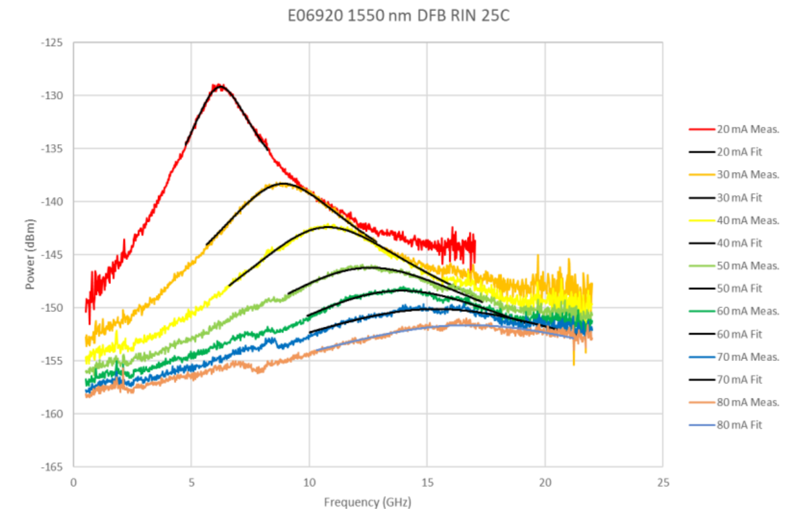
High performance wireless/photonic interfaces for 60 GHz radio over fibre applications"

- $10Gbs^{-1}$ DFB laser designed, fabricated and characterized at CST
- Cavity length: 200µm, Operation wavelength: 1550nm
- S21 3dB Bandwidth: 14GHz (25C), Output Power: 10dBm (50mA, 25C)









1270nm GPON DFB Lasers

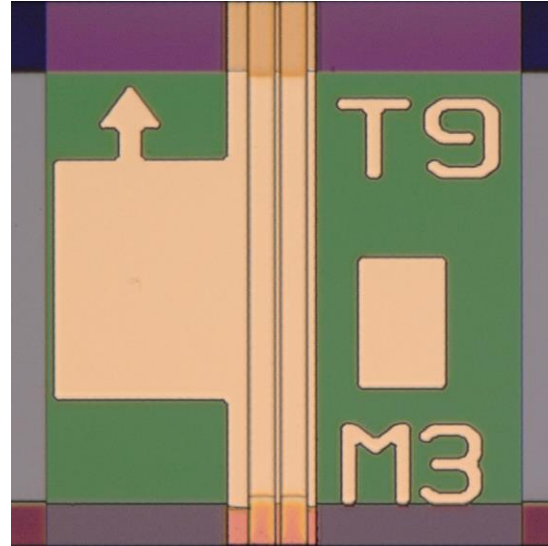
ITU XG-PON (G.987.2 - 2.5G)

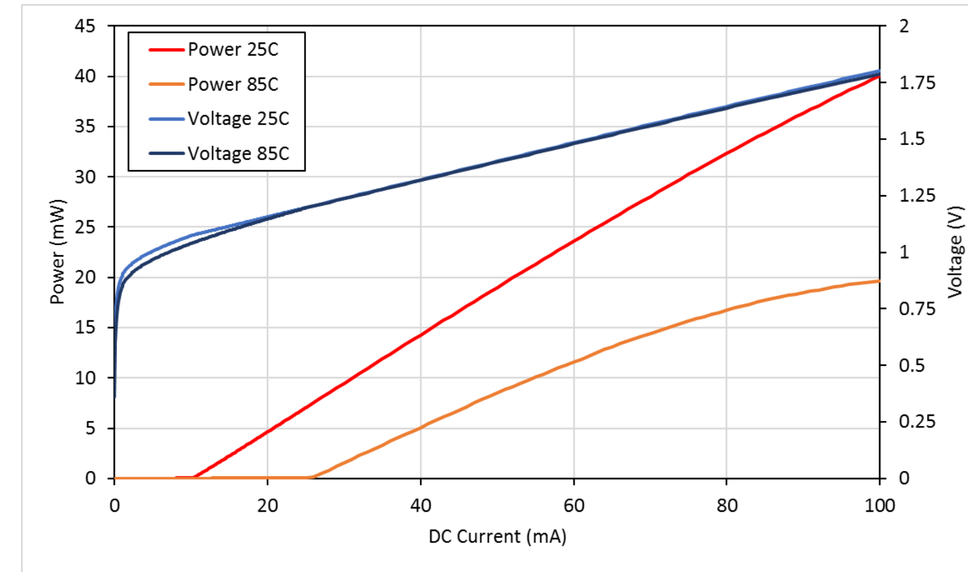
ITU-XGS-PON (G.9807.1 - 10G)

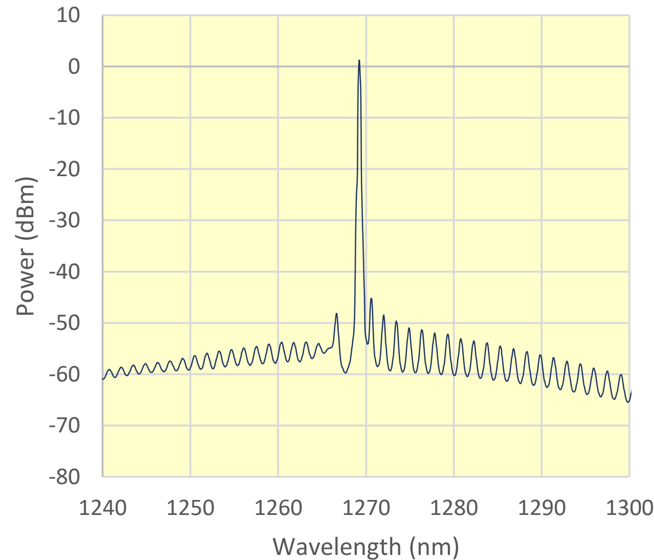
(Rated from -40C to +85C)

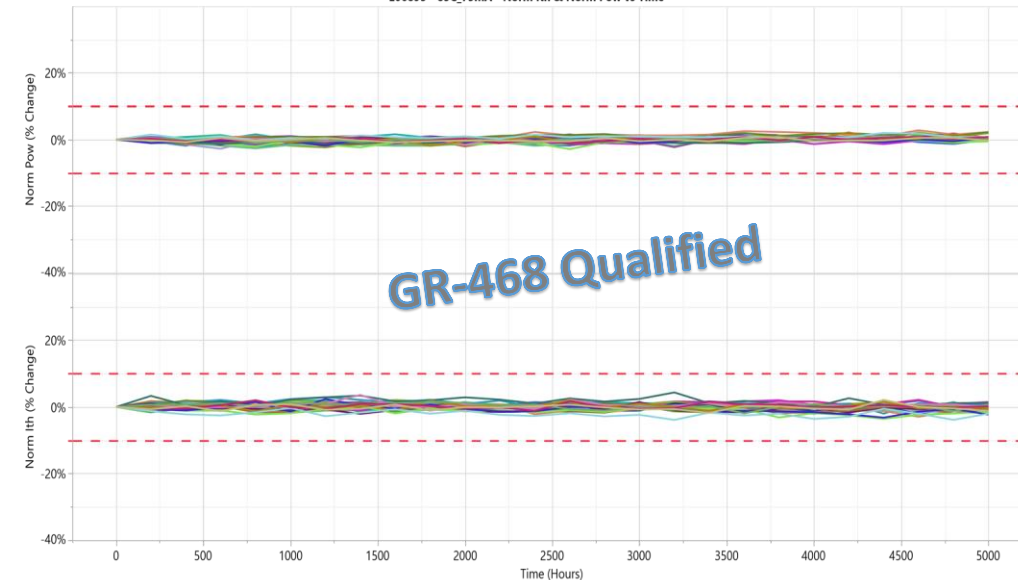
COMPOUND SEMICONDUCTOR TECHNOLOGIES

- 2.5G/10G DFB lasers designed, fabricated and qualified







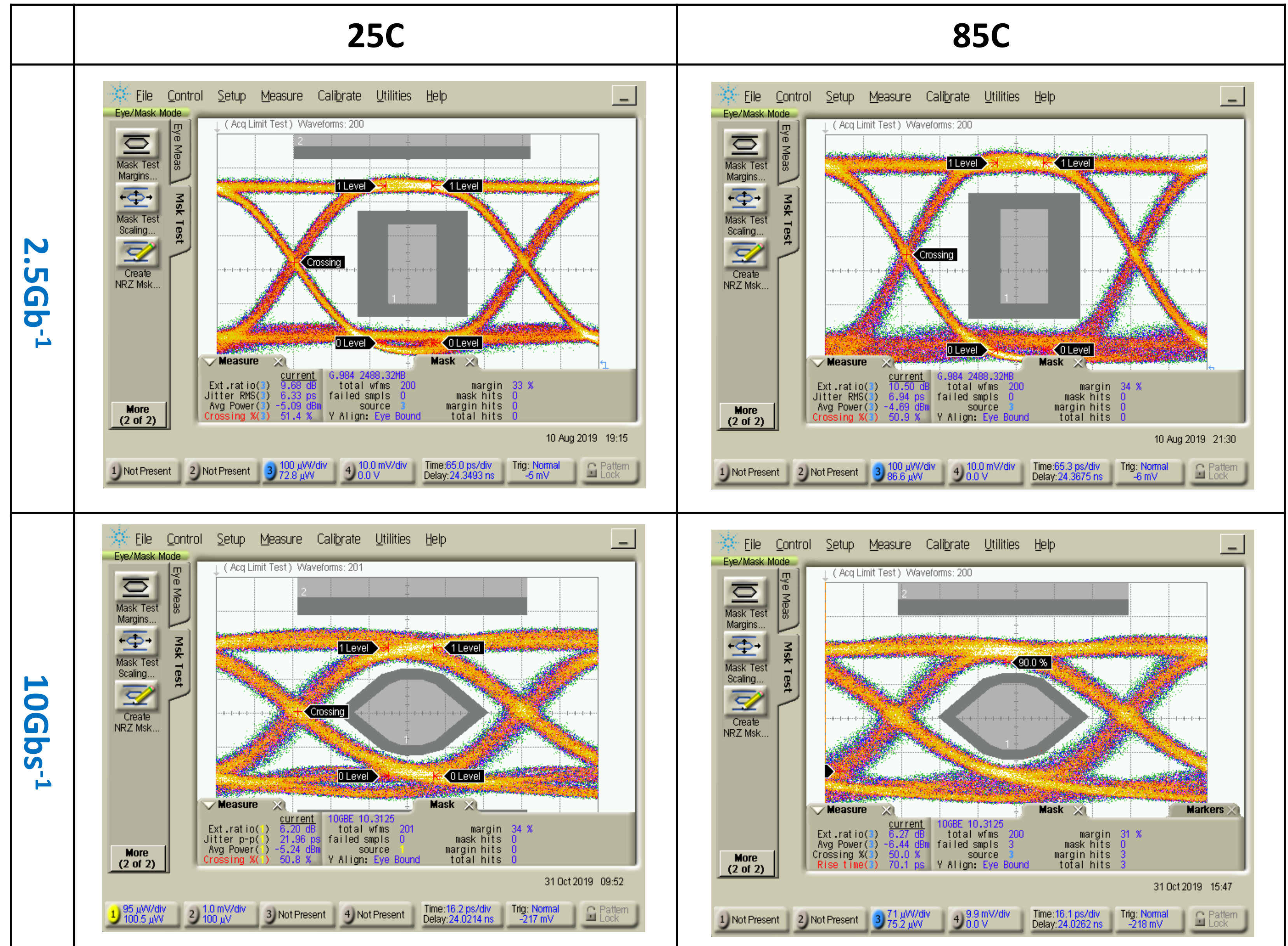


• 1270nm GPON DFB Lasers

ITU XG-PON (G.987.2 - 2.5G)

ITU-XGS-PON (G.9807.1 - 10G)

• NRZ eye diagrams of lasers in high-speed TOSA packages.



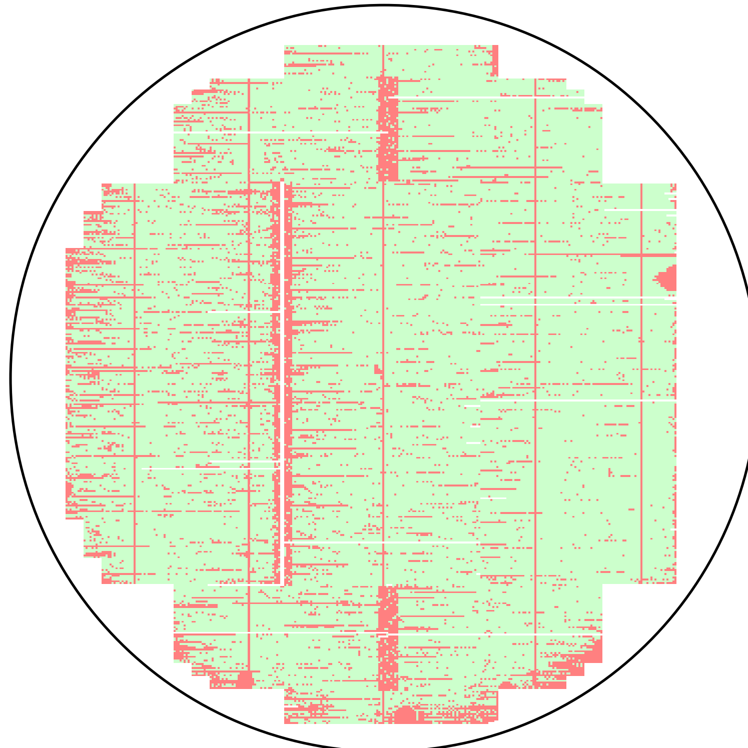
COMPOUND SEMICONDUCTOR TECHNOLOGIES

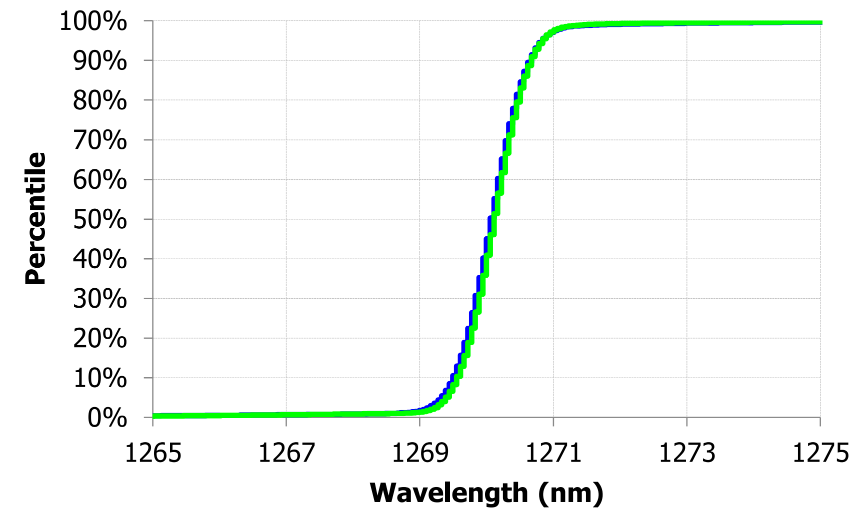
• 1270nm GPON DFB Lasers

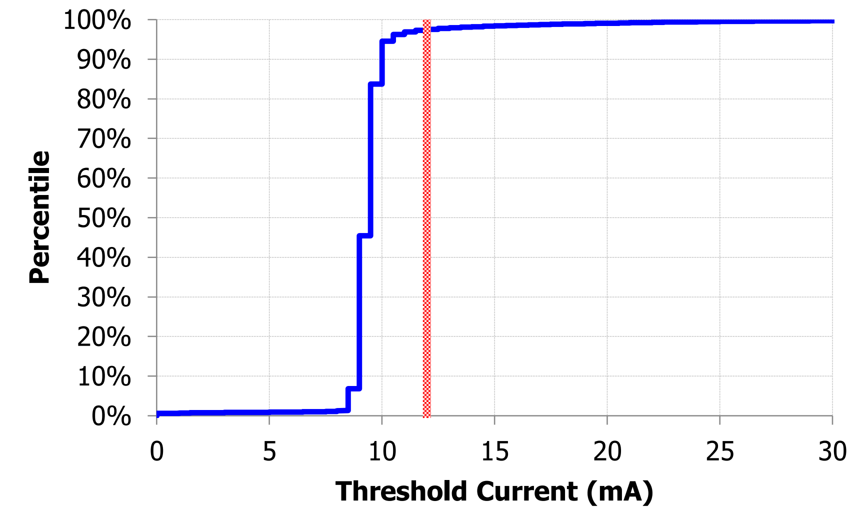
ITU XG-PON (G.987.2 - 2.5G)

ITU-XGS-PON (G.9807.1 - 10G)

- Very Uniform Gratings and ridge process control leading to very accurate lasing wavelength and uniformity.
- 90,000 die sites per 100mm wafer
- Wavelength range +/- 1nm.
- Ith range +/- 1mA
- >65% Test Yield







COMPOUND SEMICONDUCTOR TECHNOLOGIES

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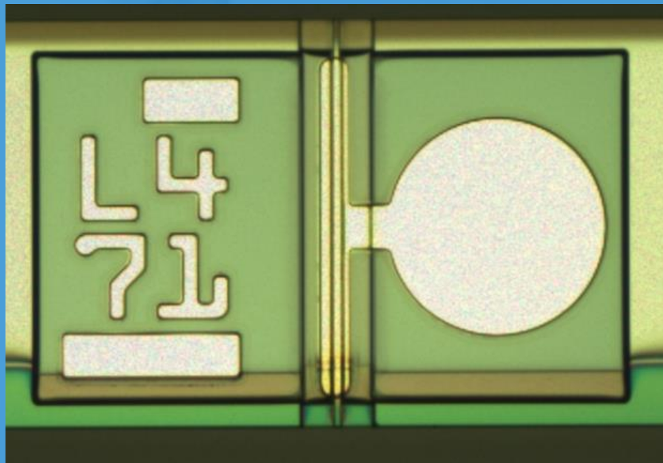
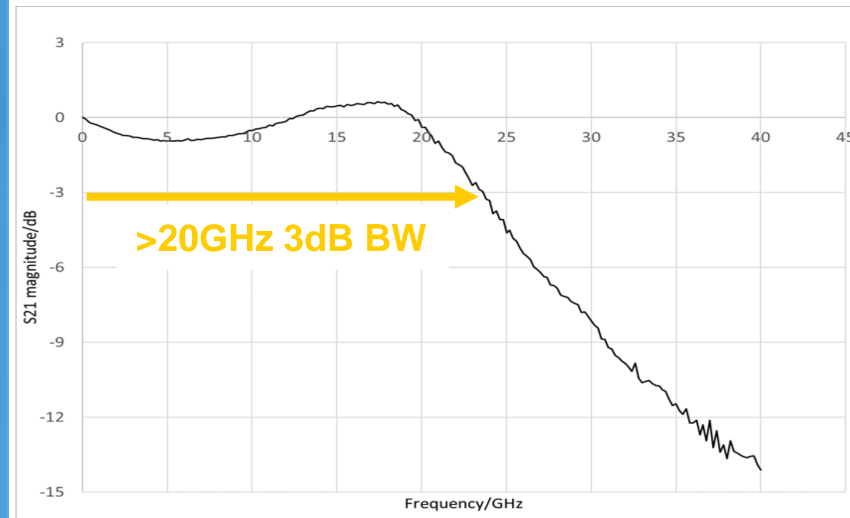
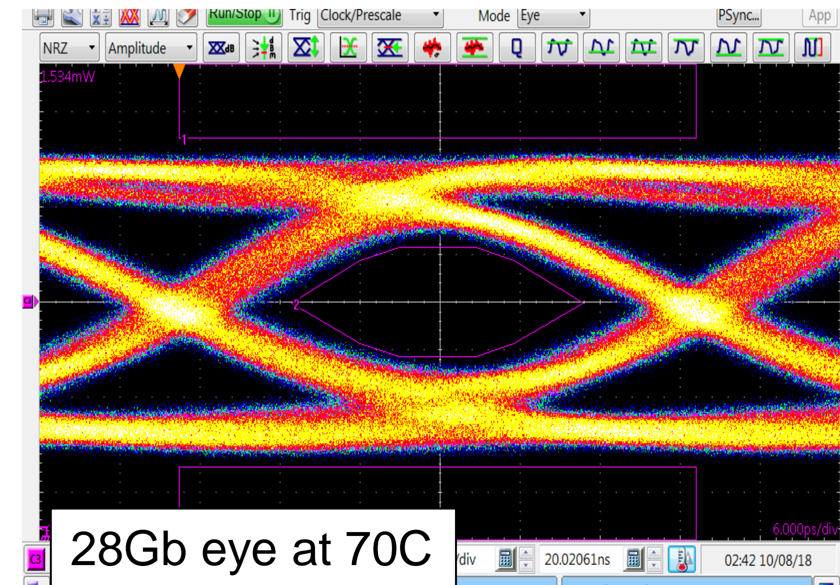
• O-band 25G DFB Lasers

CWDM channels (1270,1290,1310,1330)



- High resonance frequencies achieved by:
  - High differential gain
  - High number of QWs
  - High kappa gratings
  - Optimised detuning for high temp
  - Short cavity length
- Minimisation of chip parasitics
  - Minimal metal pad and track dimensions
  - Thick dielectric passivation

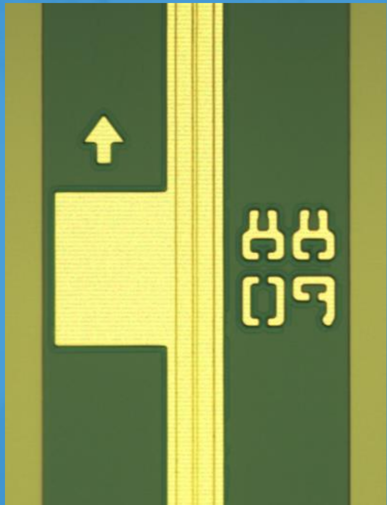




COMPOUND SEMICONDUCTOR TECHNOLOGIES

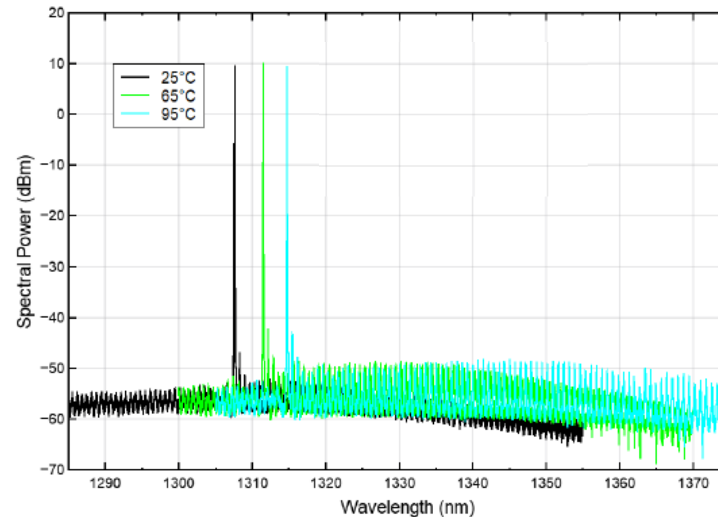
CST Public

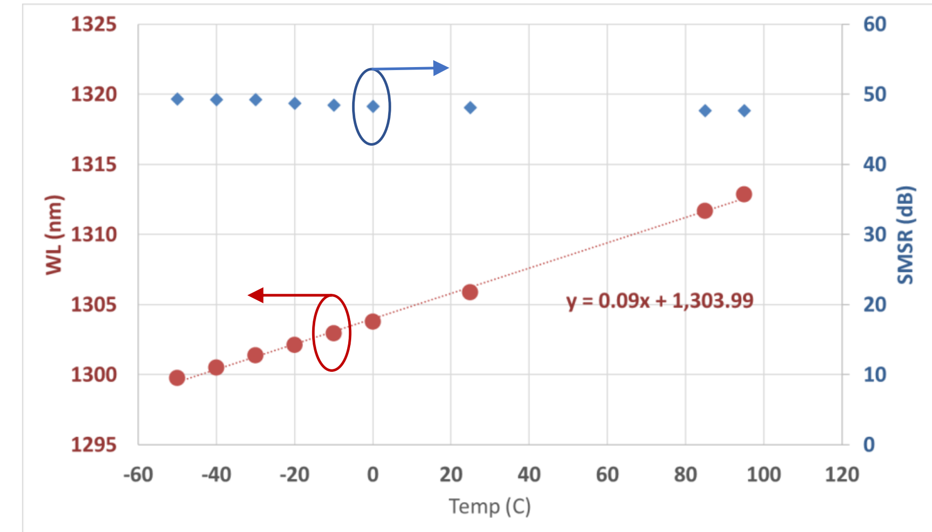
- # Wide operating temperature 1310nm DFB (for 5G LTE)



COMPOUND SEMICONDUCTOR TECHNOLOGIES

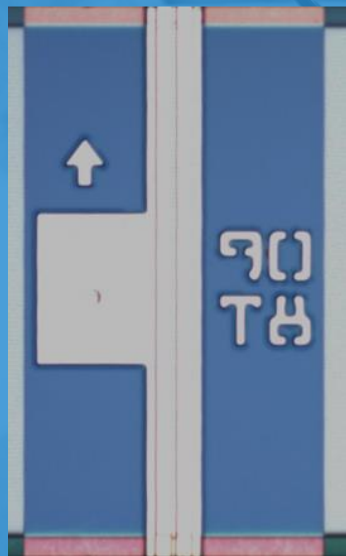
- Designed for CW operation at 25mW ex-facet output power.
- Functional from -50C to +95C assembled in TOSA packages.
- Performance achieved through:-
  - Optimised MQW active region, grating design, and cavity length.



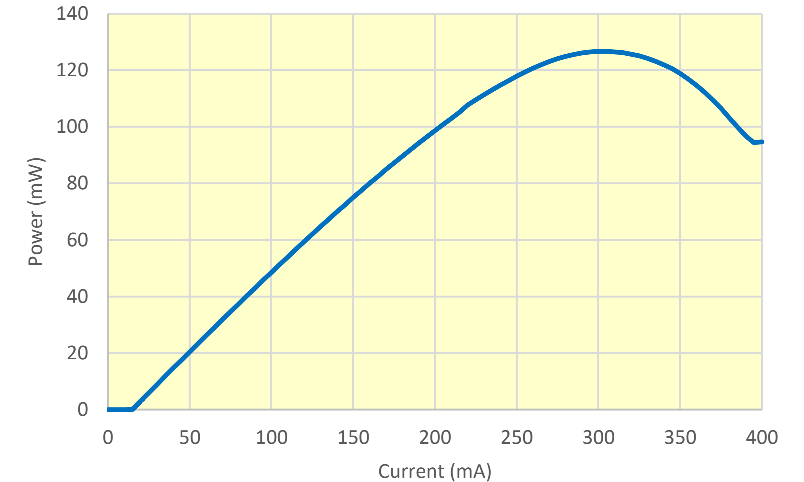


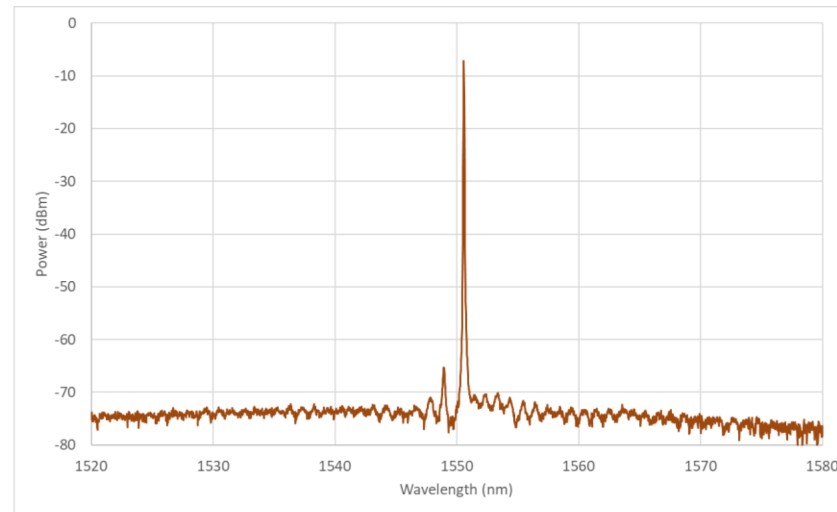
CST Public

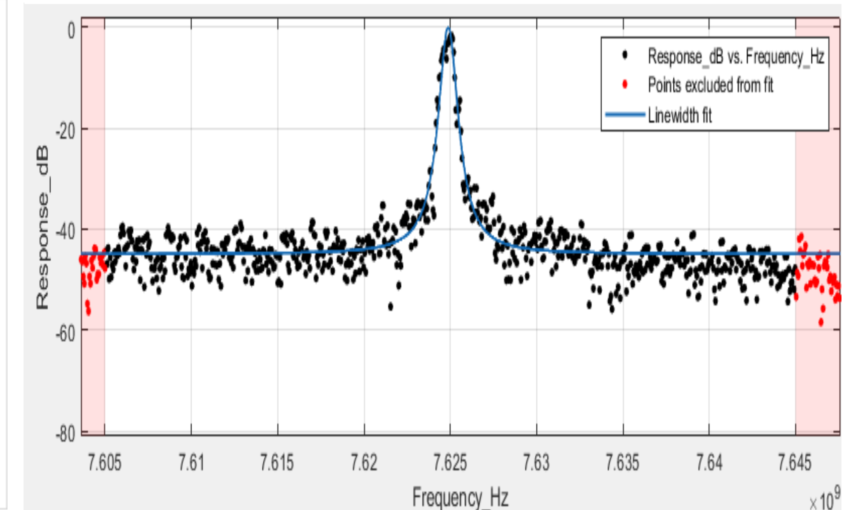
• High Power 1550nm DFB for LIDAR



- Existing 100mW output at 25C. Higher powers achievable through further optimised epi/grating designs for longer cavity lasers.
- LWs down to <300kHz range.
- SMSR > 50dB.





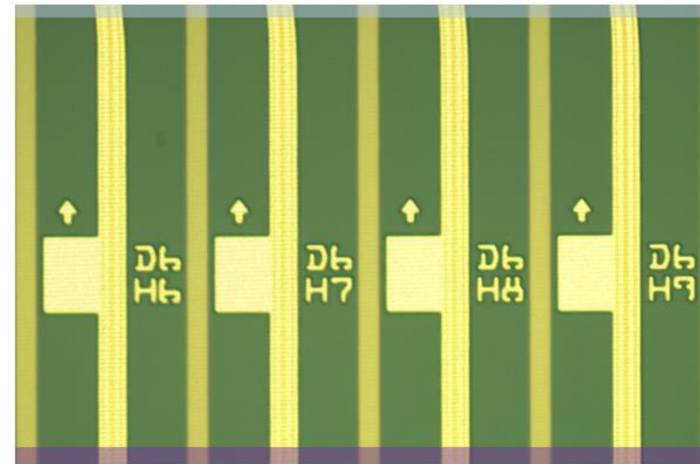


COMPOUND SEMICONDUCTOR TECHNOLOGIES

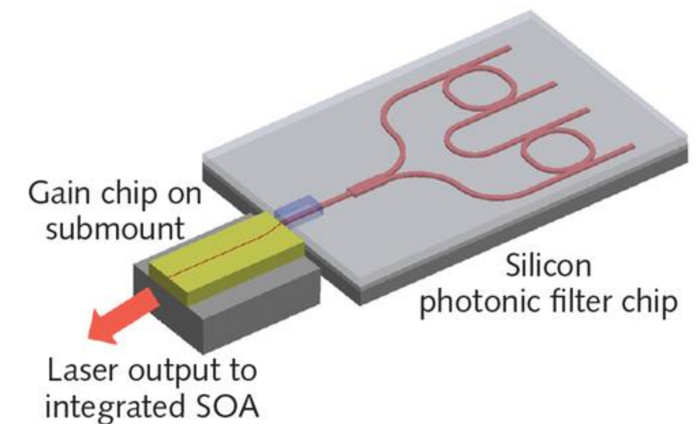
• RSOA (Gain Blocks) for tuneable lasers

- Broad gain spectra from AlInGaAs MQW active regions
- Various external cavity configurations supported
- Typical High Reflectivity (~95%) back facet
- Angled output facet to minimise reflectivity (-50dB)
- Typical external cavity laser performance of 50mW at 55C over 40nm tuning range
- Supplied as single or, more commonly, array format

AR facet (-50dB)



HR facet (~95%)



COMPOUND SEMICONDUCTOR TECHNOLOGIES

CST Public

InP100 Platform Summary

- The platform can support a number of end applications via a very broad range of laser designs:
    - rf
    - Comms, Datacenter, 5G
    - LIDAR
    - Sensing
  - High Power DFBs (>100mW, >20dBm)
  - High Speed DFBs (>20GHz 3dB BW)
  - Narrow Linewidth DFBs (<300kHz)
  - Wide Operating Temperature Range (-50C to +95C)
  - High parametric test yields (>65% on 1270nm GPON)
  - Excellent cross-wafer parametric uniformity (eg +/- 1nm wavelength)
  - Proven High Reliability (5,000hrs GR-468 qualification)
  - Scalable to high volume capacity

  - *Complete in-house capability: design, fabrication, test, reliability and qualification.*

COMPOUND SEMICONDUCTOR TECHNOLOGIES

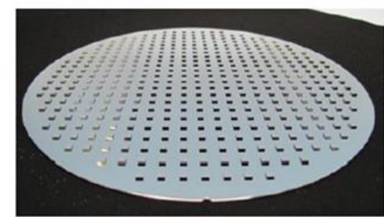
Silicon Photonics

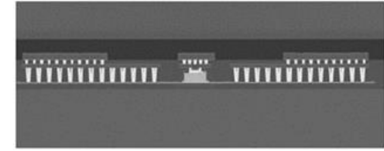
- Landscape

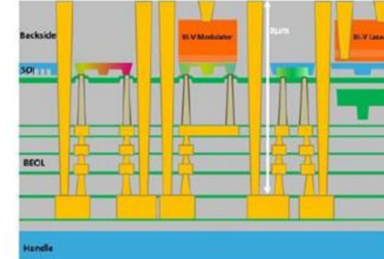
- Data comms and 5G
- Spectroscopic sensing
- Bio-Sensing
- LIDAR

COMPOUND SEMICONDUCTOR TECHNOLOGIES

- Silicon Photonics
  - Example circuits

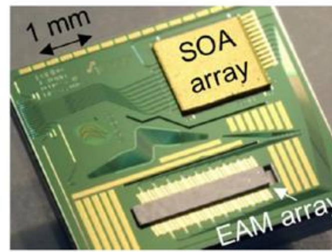

Die Bonding on 200 & 300mm Si wafers


III-V/Si Laser with multilevel planar BEOL

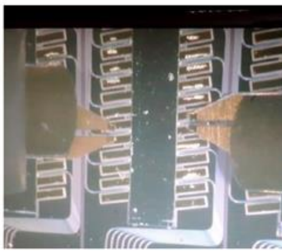


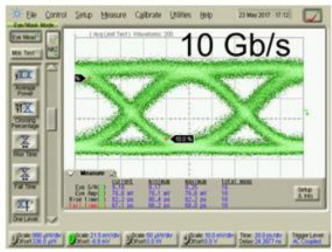
III-V/Si components integrated on backside of a complex photonic platform

cea leti

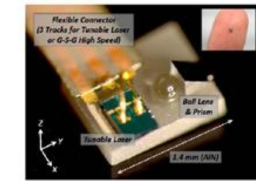


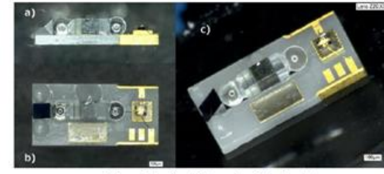
5x5 mm SOI chip with 8-ch SOA and EAM arrays


EAM array being tested on SOI



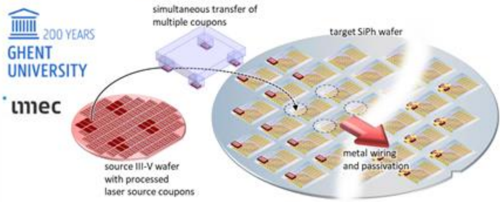
InP EAM test result

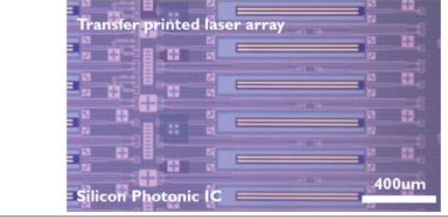

Standard Micro Optical Bench



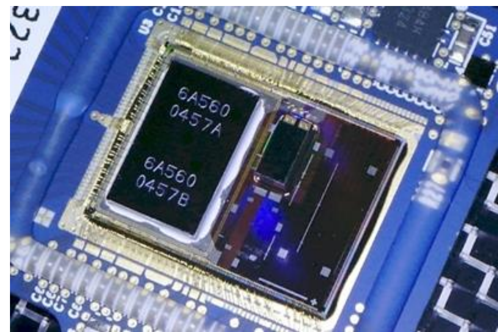
Micro Optical Bench with Isolator

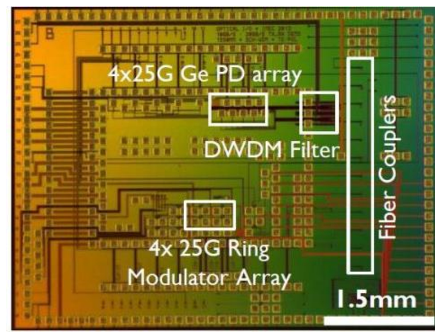
Transfer printing





ePIXfab The European Silicon Photonics Alliance http://epixfab.eu





COMPOUND SEMICONDUCTOR TECHNOLOGIES

CST Public

• Silicon Photonics

- Fabs

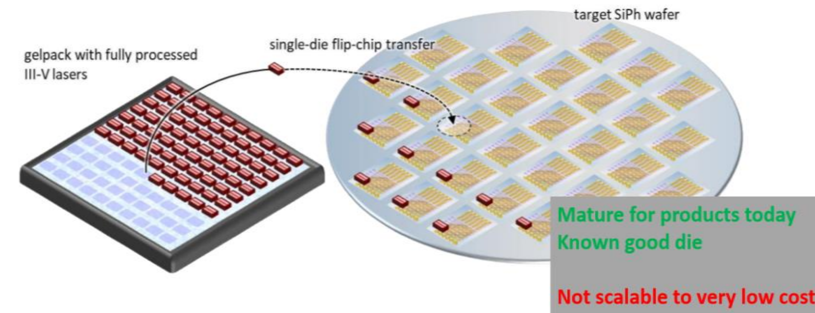
Table 1 Prominent Open-Access Silicon Photonics Technology Platforms Offered by Various Fabs, Their Technology, and Access Mechanism

Foundry	Platform	Technology	Access	Waveguide Layer Thickness (nm)	Wafer Size (inch)
		RAPID PROTOTYPING SERVICES			
AMO	thin SOI SiN	e-beam	Direct	220, 340	6
Applied Nano Tool	thin SOI	e-beam	Direct	220, 300	6
CNM/VLC	SiN	e-beam	Direct	300	4
Cornerstone	thin SOI	248 nm	Direct	220, 340, 500	8
LIGENTEC	SiN	-	Direct	up to 2500	4/6
		CMOS PILOT LINES & RESEARCH INSTITUTES			
AIM (SUNY)	thin SOI SiN	- -	MOSIS	- -	12 12
CEA-LETI	thin SOI Ge/SiGe	193 nm	CMP	310 up to 3000	8 8
IHP	SiGe BiCMOS	248 nm	Europractice	220	8
IMEC	thin SOI SiN	193 nm	Europractice Direct	220	8 8
IMECAS	thin SOI	-	SPP	220	8
INPHOTEC	thin SOI	e-beam	Direct	220	6/8
Sandia Lab	thin SOI	-	Direct	240	
VTT	thick SOI	UV	Direct	3000	6
		INDUSTRIAL FABS			
AMF(former IME)	thin SOI SiN SiN-on-SOI	248/193 nm	Direct[†]	220, 340 - -	8 8 8
CompoundTek	thin SOI	193 nm immersion	Direct	-	-
Global Foundry/IBM	thin SOI	193 nm immersion / 248 nm	MOSIS, Direct, TAPO	sub-100 nm	8/12
SilTerra	thin SOI	-	Direct	-	8
SMIC	Thin SOI	-	Direct	340	8
ST Micro[§]	thin SOI	193 nm	Direct	310	12
TowerJazz	thin SOI	193 nm	Direct	-	8
TSMC	thin SOI	-	-	-	12
LioniX	SiN	UV	Direct	flexible	-

COMPOUND SEMICONDUCTOR TECHNOLOGIES

• Integrating III-V with Silicon Photonics

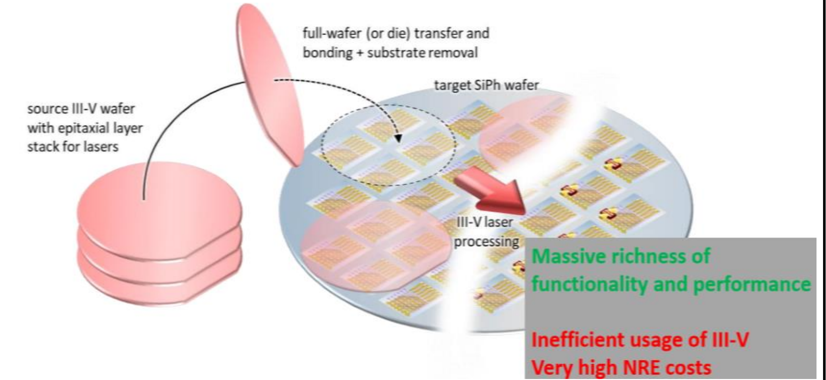
Flip-chip integration of bare dies / pick-and-place of packaged devices



Mature for products today
Known good die

Not scalable to very low cost

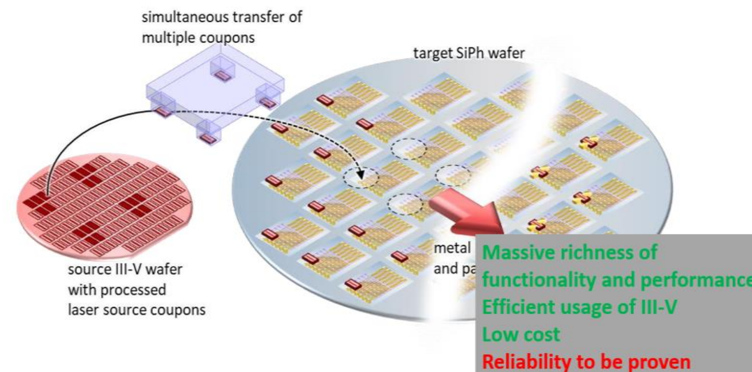
die-to-wafer and wafer-to-wafer bonding + III-V processing in silicon fab



Massive richness of functionality and performance

Inefficient usage of III-V
Very high NRE costs

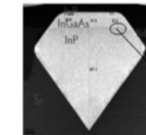
Transfer printing

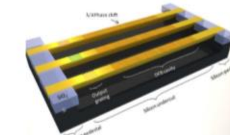


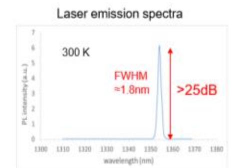
Massive richness of functionality and performance
Efficient usage of III-V
Low cost
Reliability to be proven

III-V on Silicon Hetero-Epitaxy

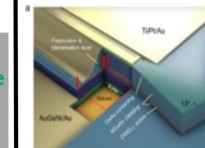
O-pumped InP DFB lasers (RT) @ imec

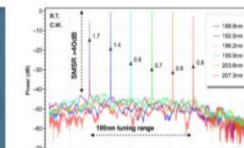




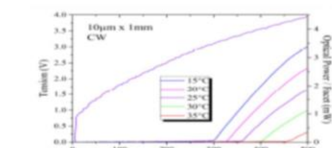


E-pumped QD DFB lasers (RT, CW) @ UCL





E-pumped GaSb QW lasers (RT) @ U.Montpellie



Remaining big challenge: integration in the SiPh process flow

COMPOUND SEMICONDUCTOR TECHNOLOGIES

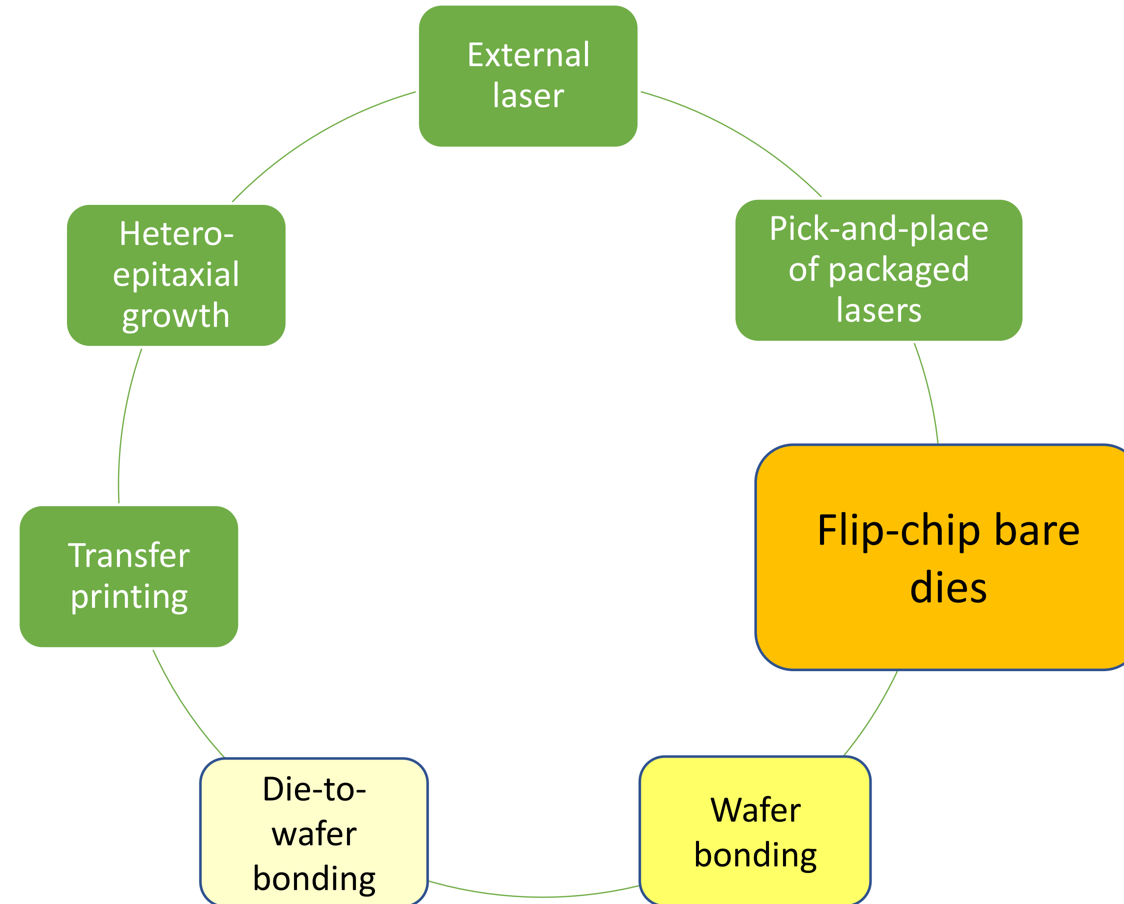
Prof. Roel Baets

GHENT UNIVERSITY imec

- Integrating III-V with Silicon Photonics

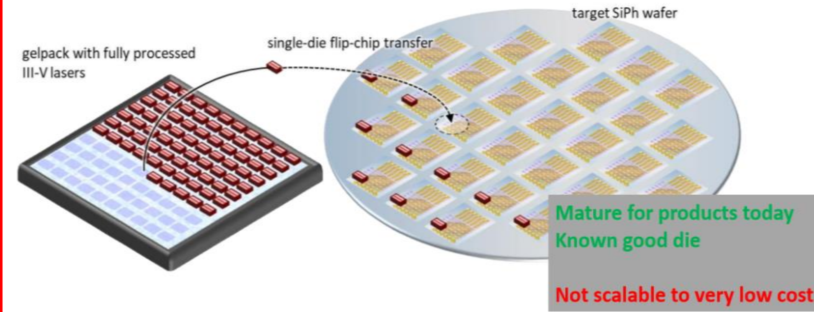
COMPOUND SEMICONDUCTOR TECHNOLOGIES

- Where does CST fit-in?

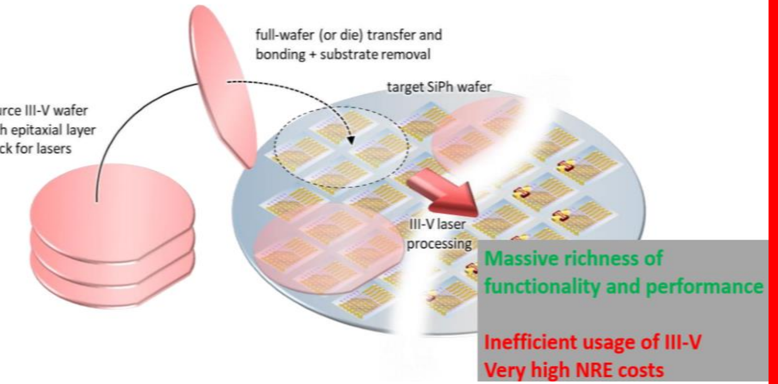


• Integrating III-V with Silicon Photonics

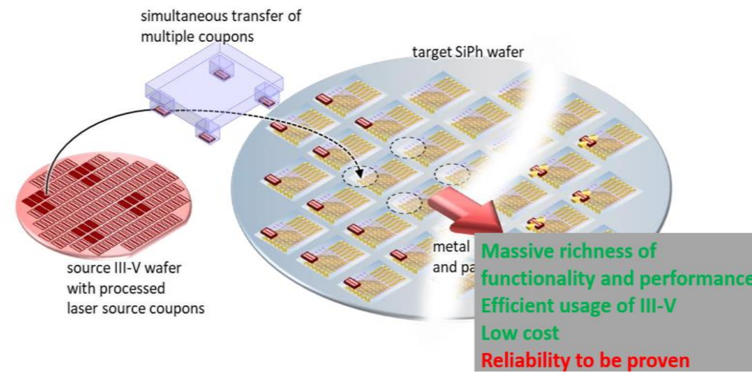
Flip-chip integration of bare dies / pick-and-place of packaged devices



die-to-wafer and wafer-to-wafer bonding + III-V processing in silicon fab

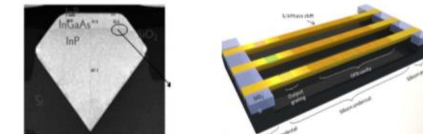


Transfer printing

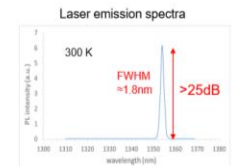


III-V on Silicon Hetero-Epitaxy

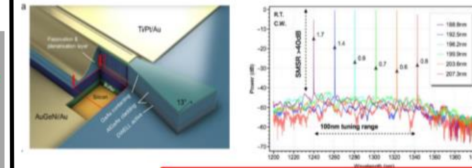
O-pumped InP DFB lasers (RT) @ imec



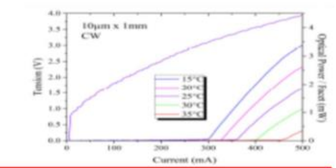
Laser emission spectra



E-pumped QD DFB lasers (RT, CW) @ UCL



E-pumped GaSb QW lasers (RT) @ U.Montpellie

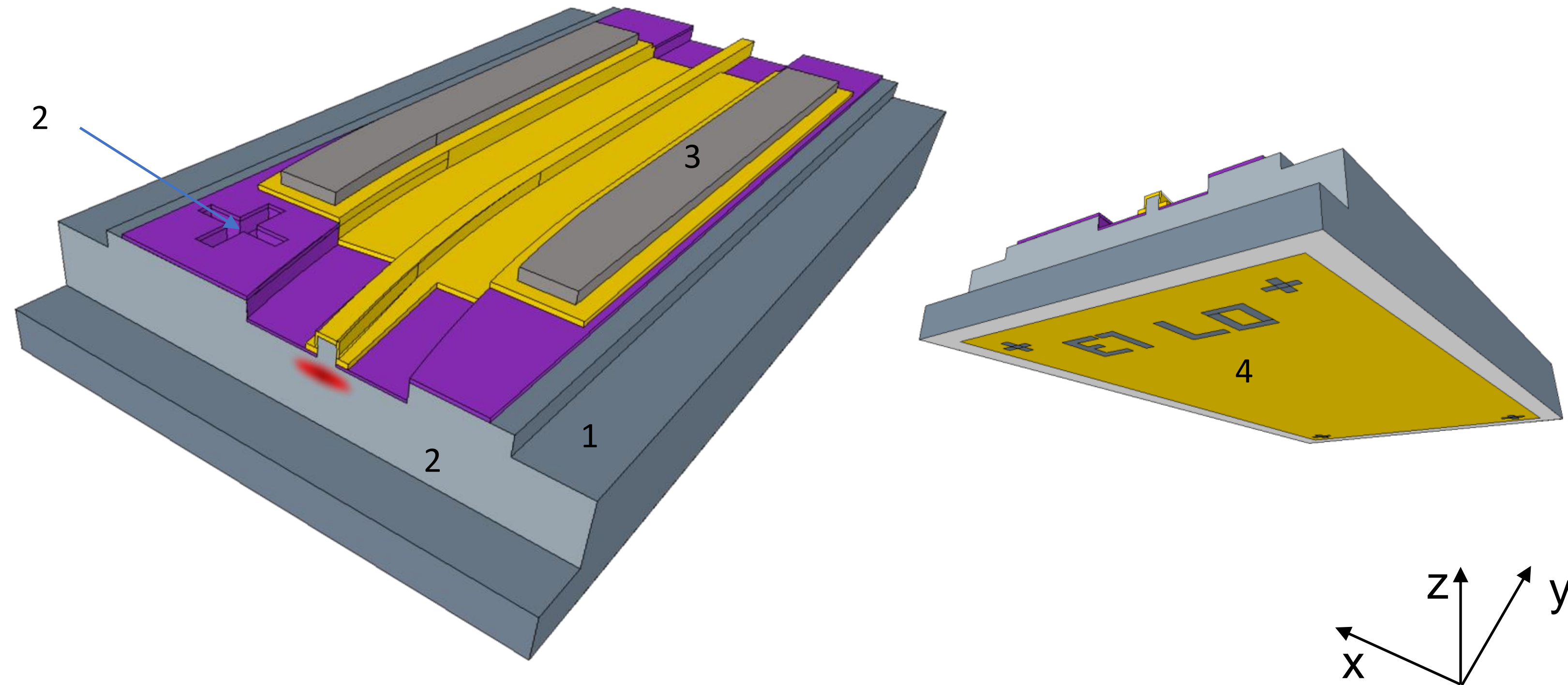


Remaining big challenge: integration in the SiPh process flow

COMPOUND SEMICONDUCTOR TECHNOLOGIES

InP RSOA chip optimised for Flip-Chip Assembly to SiPh

- Connection Details of InP100 to SiPh
  - Example Device



Key design features:

1. Vertical alignment surfaces. +/- 5nm height accuracy to optical mode centre. (z-axis)
2. Etched facet with self-aligned front-side fiducials to both ridge (x-axis) and facet (y-axis).
3. Metal pads for flip chip bonding. AuSn solder optional.
4. Backside alignment fiducials, and chip IDs.
5. Particle-free front-side.

COMPOUND SEMICONDUCTOR TECHNOLOGIES

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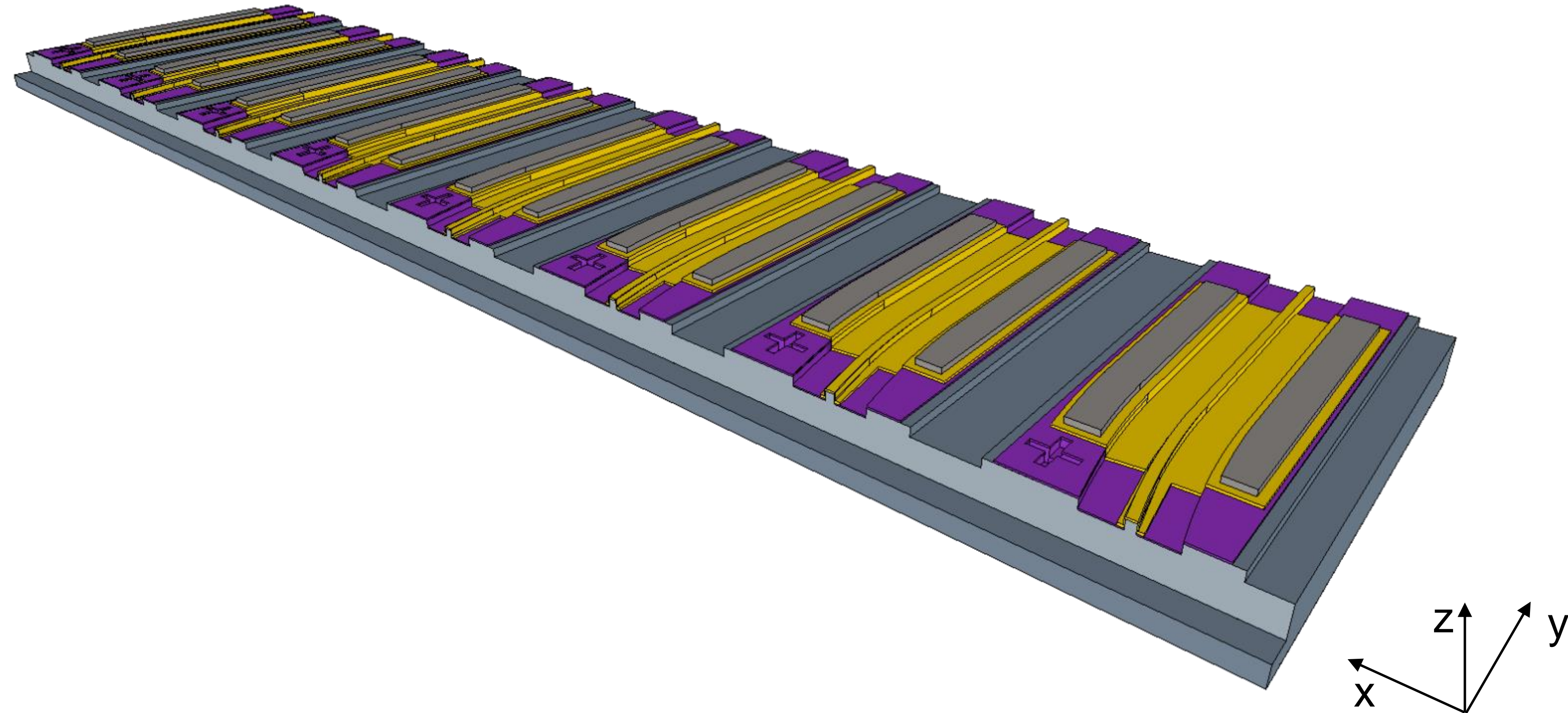
- Connection Details of InP100 to SiPh

  - Example Device

COMPOUND SEMICONDUCTOR TECHNOLOGIES

InP RSOA ***8x-array*** optimised for Flip-Chip Assembly to SiPh



Key design features:

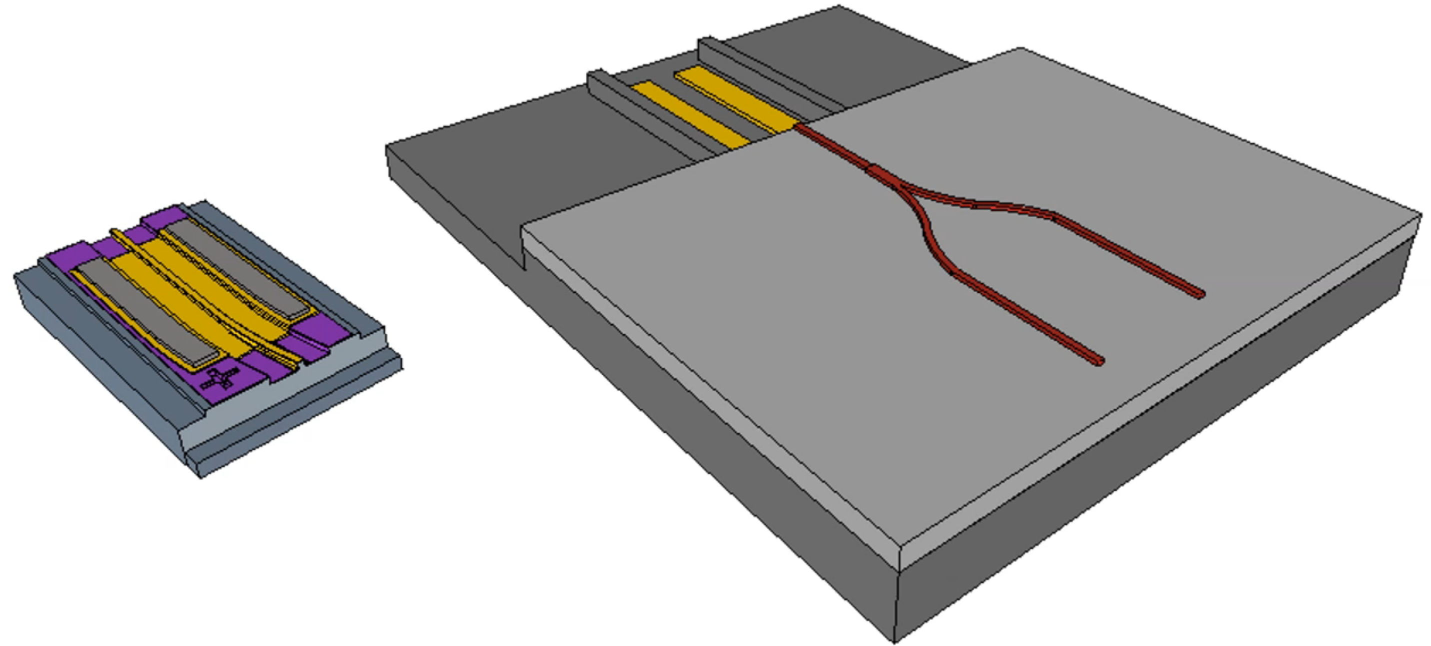
1. Vertical alignment surfaces. +/- 5nm height accuracy to optical mode centre. (z-axis)
2. Etched facet with self-aligned front-side fiducials to both ridge (x-axis) and facet (y-axis).
3. Metal pads for flip chip bonding. AuSn solder optional.
4. Backside alignment fiducials, and chip IDs.
5. Particle-free front-side.
6. Single chips or multi-channel arrays

CST Public

- Connection Details of InP100 to SiPh

- Integration Process

InP RSOA chip Flip-Chipped onto SiPh



Key design features:

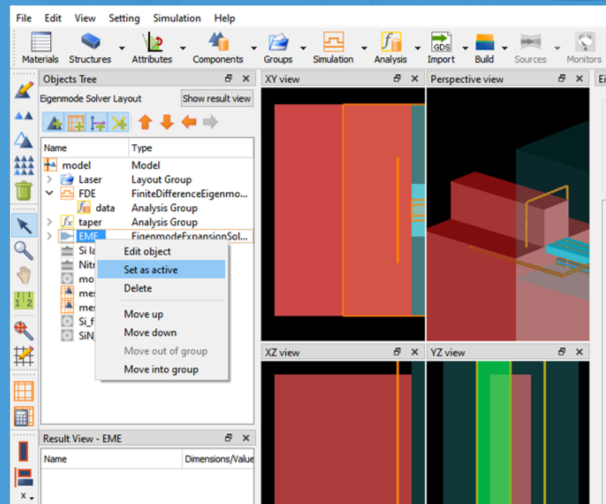
1. Vertical alignment surfaces. +/- 5nm height accuracy to optical mode centre. (z-axis)
2. Etched facet with self-aligned front-side fiducials to both ridge (x-axis) and facet (y-axis).
3. Metal pads for flip chip bonding. AuSn solder optional.
4. Backside alignment fiducials, and chip IDs.
5. Single chips or multi-element arrays

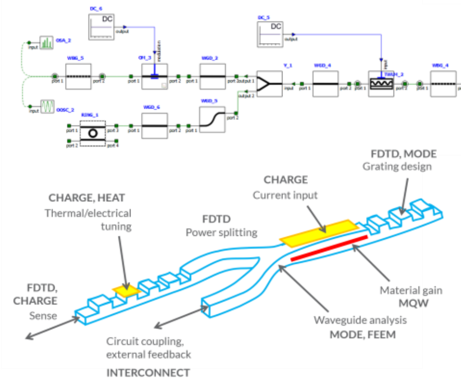
COMPOUND SEMICONDUCTOR TECHNOLOGIES

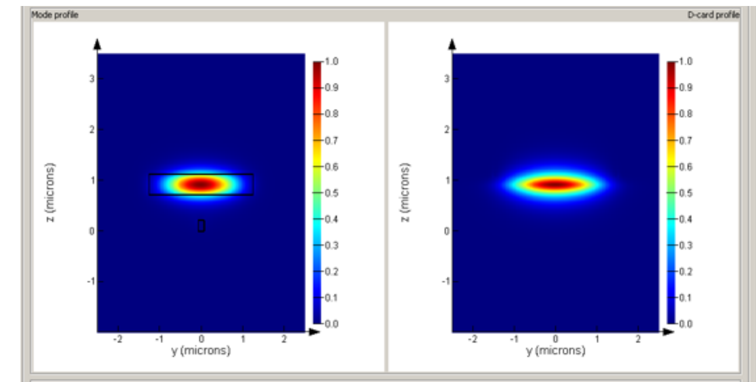
CST Public

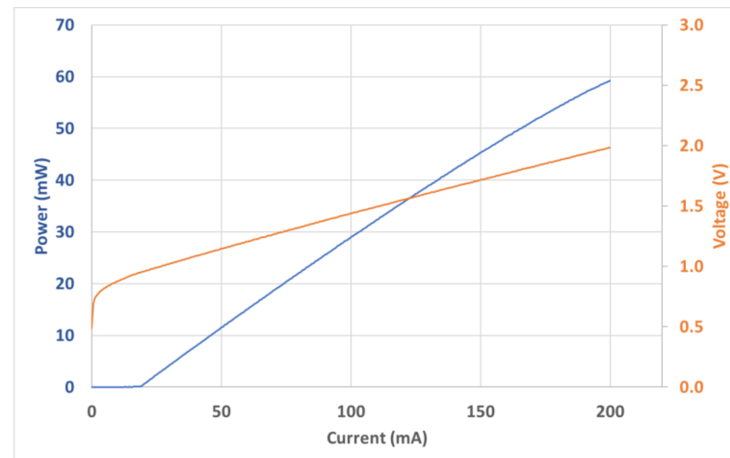
Accessing the InP100 platform using a PDK

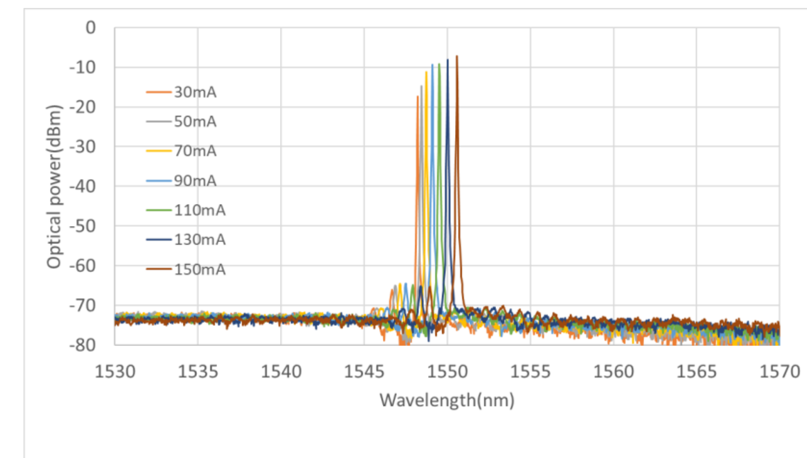
- InP100 PDK is under development with Cadence and Lumerical
- Ongoing development on the modelling (simulation) and physical co-design (ie, footprint, package) sides
- Workshop example to include CST 1550nm DFB laser











COMPOUND SEMICONDUCTOR TECHNOLOGIES

CST Public

Summary

- Discussed CST's InP100 platform and demonstrated the various high performance laser sources that can be fabricated from it, including lasers for rf-photonics applications.

- Discussed how CST lasers support the SiPh eco-system and where it's technology for III-V hybrid integration is specifically used.

- *Complete in-house capability: design, fabrication, test, reliability and qualification.*

COMPOUND SEMICONDUCTOR TECHNOLOGIES

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Thank You !!